VARIOUS STRUCTURE/HEIGHT BUMPS FOR WAFER LEVEL-CHIP SCALE PACKAGE

FIELD OF THE INVENTION

The present invention relates generally to fabrication of semiconductor chip interconnection, and more specifically to bump fabrication for wafer level-chip scale packages (WL-CSP).

BACKGROUND OF THE INVENTION

Improvements to bumps for wafer level-chip scale packages (WL-CSP) are needed.

U.S. Patent No. 6,486,054 B1 to Fan et al. describes a method to achieve robust solder bump height.

U.S. Patent No. 6,184,581 B1 to Cornell et al. describes a solder bump input/output pad for a surface mount circuit device with adjacent input/output pads also having triangular shapes or diamond shapes.

U.S. Patent No. 5,926,731 to Coapman et al. describes a method for controlling solder bump shape and stand-off height.

U.S. Patent No. 6,297,551 B1 to Dudderar et al. describes integrated circuit packages with improved EMI characteristics.

U.S. Patent No. 4,430,690 to Chance et al. describes a low inductance MLC capacitor with metal impregnation and solder bar contact.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved bump design for wafer level-chip scale packages.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a die comprising: a substrate; two or more various shaped bump structures having a solder line formed over the substrate; and an epoxy layer formed over the substrate. The epoxy layer having a top surface wherein: (a) the solder lines are below the top surface of the epoxy layer'; (b) the solder lines are above the top surface of the epoxy layer; or (c) some of the solder lines are below the top surface of the epoxy layer and some of the solder lines are above the top surface of the epoxy layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 and 2 schematically illustrate a first preferred embodiment of the present invention having the epoxy above the solder line with Fig. 1 being a cross-sectional view of Fig. 2 along line 1-1.

Figs. 3 and 4 schematically illustrate a second preferred embodiment of the present invention having the epoxy below the solder line with Fig. 3 being a cross-sectional view of Fig. 4 along line 3-3.

Figs. 5 and 6 schematically illustrate a third preferred embodiment of the present invention having the epoxy above and below the solder line with Fig. 5 being a cross-sectional view of Fig. 6 along line 5-5.

Figs. 7 to 15 schematically illustrate the formation of a wafer level-chip scale package (WL-CSP) formed in accordance with the method of the present invention.

Fig. 16 schematically illustrates stacked die/chip mounting with variable height bumps.

Fig. 17 schematically illustrates a flip chip mounted to a dual height substrate with variable height bumps.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment: Epoxy Layer 22' Above the Solder Lines 14 – Figs. 1 and 2

As shown in Fig. 1, in the first embodiment of the present invention, the top of the epoxy layer 22' is above the respective solder lines 14 of the various shaped bumps structures 11, 15, 17, 19 formed over the die/chip substrate 10.

Epoxy layer 22' is preferably comprised of thermosetting resins or an underfill coating material.

Fig. 2 is a top down view of Fig. 1, with Fig. 1 being a cross-sectional view of Fig. 2 at line 1-1.

In the present invention, and again as more clearly shown in Fig. 2, the bump structures 11, 15, 17, 19 are of various shapes. For example the bump structures 11, 15, 17, 19 may be:

a) round bump structures 11 having a diameter of preferably from about 40 to 300μm;) wall bump structures 16 forming, for example a square or rectangle, and having a width of preferably from about 40 to 300μm and more preferably from about 100 to 200 μm ; and, if rectangular, a length of preferably from about 300 to 3000μm and more preferably from about 350 to 1200 μm;

c) bar bump structures 18 having a width of preferably from about 40 to 300μm and having a length of up to about 3000μm and more preferably about 1500μm that have excellent current carrying capacity; or

d) circular bump structures 19 having an outside diameter of preferably from about 150 to 3000μm and an inside diameter of preferably from about 100 to 2500μm.

Each bump structure 11, 15, 17, 19 includes respective solder 12, 16, 18, 20 thereover defining the solder lines 14. For the wall bump structures 16 forming, for example a square or rectangle, the square or rectangular structure may include internal (as shown in Fig. 2) or external bump structures 12'.

It is noted that other shapes are also possible.

These various shaped bump structures 11, 15, 17, 19 provide for enhanced electrical or thermal performance. A square or rectangle wall bump structure 16, for example, could be used as shielding for RF applications, e.g.: internal I/O may be noise sensitive; or RF shield, or a Faraday cage.

While Fig. 2 more clearly illustrates the various shapes of the bump structures 11, 15, 17, 19, Fig. 2 illustrates only a sample combination of such bump structures 11, 15, 17, 19 and does not limit the scope of the present invention.

Second Embodiment: Epoxy Layer 22'' Below the Solder Lines 14 – Figs. 3 and 4

As shown in Fig. 3, in the second embodiment of the present invention, the top of the epoxy layer 22'' is below the respective solder lines 14 of the various shaped bumps structures 11, 15, 17, 19 formed over the die/chip substrate 10.

Epoxy layer 22'' is preferably comprised of thermosetting resins or underfill coating material.

Fig. 4 is a top down view of Fig. 3, with Fig. 3 being a cross-sectional view of Fig. 4 at line 3-3.

In the present invention, and again as more clearly shown in Fig. 4, the bump structures 11, 15, 17, 19 are of various shapes. For example the bump structures 11, 15, 17, 19 may be:

a) round bump structures 11 having a diameter of preferably from about 40 to 300μm;b) wall bump structures 16 forming, for example a square or rectangle, and having a width of preferably from about 40 to 300μm and more preferably from about 100 to 200μm; and, if rectangular, a length of preferably from about 300 to 3000 μm and more preferably from about 350 to 1200 μm;

c) bar bump structures 18 having a width of preferably from about 40 to 300μm and having a length of up to about 3000μm and more preferably about 1500 μm that have excellent current carrying capacity; or

d) circular bump structures 19 having an outside diameter of preferably from about 150 to 3000 μm and an inside diameter of preferably from about 100 to 2500μm.

Each bump structure 11, 15, 17, 19 includes respective solder 12, 16, 18, 20 thereover defining the solder lines 14. For the wall bump structures 16 forming, for example a square or rectangle, the square or rectangular structure may include internal (as shown in Fig. 4) or external bump structures 12'.

It is noted that other shapes are also possible.

These various shaped bump structures 11, 15, 17, 19 provide for enhanced electrical or thermal performance. A square or rectangle wall bump structure 16, for example, could be used as shielding for RF applications, e.g.: internal I/O may be noise sensitive; or RF shield, or a Faraday cage.

While Fig. 4 more clearly illustrates the various shapes of the bump structures 11, 15, 17, 19, Fig. 4 illustrates only a sample combination of such bump structures 11, 15, 17, 19 and does not limit the scope of the present invention.

Third Embodiment: Epoxy Layer 22' Below Solder Lines 214' and Above Solder Lines 214'' – Figs. 5 and 6

It is noted that for stacked die or multi-tier substrates such as IC or MEMS applications, it is essential that the various shaped bump structures 211, 215, 217, 219 (11, 15, 17, 19) have two sets of heights.

As shown in Fig. 5, in the third embodiment of the present invention, the various shaped bumps structures 211, 215, 217, 219 comprise a first set of various shaped bumps structures 215, 217, 219 having a first height and a second set of various shaped bumps structures 211 having a second height that is less than the first height and thus, the top surface of the epoxy layer 22''' is below solder lines 214' of the various shaped bumps structures 215, 217, 219 and above the respective solder lines 214'' of the various shaped bumps structures 211 with each of the

various shaped bumps structures 211, 215, 217, 219 formed over the die/chip substrate 10.

It is noted that the top of the epoxy layer 22''' may be above/below any combination of the various shaped bumps structures 211, 215, 217, 219 as desired and Figs. 5 and 6 illustrate just one example combination.

Epoxy layer 22''' is preferably comprised of thermosetting resin or underfill coating material.

Fig. 5 is a top down view of Fig. 6, with Fig. 5 being a cross-sectional view of Fig. 6 at line 5-5.

In the present invention, and again as more clearly shown in Fig. 6, the bump structures 211, 215, 217, 219 are of various shapes. For example the bump structures 211, 215, 217, 219 may be:

a) round bump structures 211 having a diameter of preferably from about 40 to 300μm;b) wall bump structures 216 forming, for example a square or rectangle, and having a width of preferably from about 40 to 300μm and more preferably from about 100 to 200μm; and, if rectangular, a length of preferably from about 500 to 3000 μm and more preferably from about 500 to 1500 μm;

c) bar bump structures 218 having a width of preferably from about 40 to 300μm and having a length of up to about 3000μm that have excellent current carrying capacity; or

d) circular bump structures 219 having an outside diameter of preferably from about 150 to 3000μm and an inside diameter of preferably from about 100 to 2500μm.

Each bump structure 211, 215, 217, 219 includes respective solder 212, 216, 218, 220 thereover defining the solder lines 214', 214''. For the wall bump structures 216 forming, for example a square or rectangle, the square or rectangular structure may include internal (as shown in Fig. 6) or external bump structures 212'.

It is noted that other shapes are also possible.

These various shaped bump structures 211, 215, 217, 219 provide for enhanced electrical or thermal performance. A square or rectangle wall bump structure 216, for example, could be used as shielding for RF applications, e.g.: internal I/O may be noise sensitive; or RF shield, or a Faraday cage.

While Fig. 6 more clearly illustrates the various shapes of the bump structures 211, 215, 217, 219, Fig. 6 illustrates only a sample combination of such bump structures 211, 215, 217, 219 and does not limit the scope of the present invention.

Sequence of Formation of Bump Structures 11, 15, 17, 19; 211, 215, 217, 219 To Form Wafer Level-Chip Scale Package 100 – Figs. 7 to 15

Figs. 7 to 15 illustrate the sequence in forming bump structures 11, 15 ,17, 19; 211, 215, 217, 219 to form a wafer level-chip scale package (WL-CSP) 100 (it

is noted that chip 100 may be a flip chip, for example). For ease of understanding and simplicity bump structures 11, 15, 17, 19; 211, 215, 217, 219 are represented by a single composite final bump structure(s) 90'''.

It is noted that Fig. 7 to 13 represent a portion of the complete wafer/die/chip substrate 10 as is shown in Fig. 14 and that Fig. 15 is a WL-CSP 100 cut from the entire wafer/die/chip substrate 10 of Fig. 14.

Fig. 7 is an overhead view of Fig. 8 with Fig. 8 being a cross-sectional view of Fig. 7 along line 8-8.

Initial Structure – Figs. 7 and 8

Figs. 7 and 8 include inchoate bump structures 90 formed over a wafer/die/chip substrate 10 that may have various initial shapes (see Figs. 1 to 6 and the descriptions herein).

Inchoate bump structures 90 each include a lower pillar metal portion 92 preferably comprised of conductive metals with non-re-flowed characteristics, the ability to be coated with other metals or high melting point characteristics and more preferably the ability to be coated with other metals and having a height of preferably from about 65 to 120μm and more preferably form about 65 to 85μm; with an upper portion 94 preferably comprised of eutectic solder or lead free solder and having a thickness of preferably from about 35 to 60μm and more preferably form about 35 to 40μm.

It is noted that, while not specifically shown in Figs. 7 to 15 for simplicity and ease of understanding, the final single composite bump structure(s) 90''' may comprise two sets of overall heights – see Figs. 5 and 6 (the third embodiment); and 16 and 17 and those relevant descriptions.

Fluxing – Fig. 9

As shown in Fig. 9 in a fluxing step, flux 96 is formed over the respective upper portions 94 to a thickness of preferably from about 1 to 10μmand more preferably from about 5 to 7μmto form first intermediate inchoate bump structures 90'. Flux 96 is preferably water soluble.

Solder/Solder Ball 98 Placement – Fig. 10

As shown in Fig. 10, respective solder/solder balls 98 is/are formed over the flux 96 to form second intermediate inchoate bump structures 90''. Solder/solder balls 98 are preferably comprised of eutectic or lead-free solder. Solder Balls 98 can also be formed using solder paste printing (eutectic or lead-free solder). No ball placement is required for solder paste.

Reflow – Fig. 11

As shown in Fig. 11, the solder/solder balls 98 are subjected to a reflow process to form reflowed solder/solder balls 98', define solder lines 14 and to form final bump structures 90'''. The reflow process is preferably at a

temperature of from about 100 to 260°C and from about 5 to 10 minutes and more preferably from about 5 to 7 minutes.

Epoxy 22 Coating – Fig. 12

As shown in Fig. 12, an initial layer of epoxy 22 is formed over the wafer/die/chip substrate 10 and the final bump structures 90''' (bump structures 11, 15, 17, 19; 211, 215, 217, 219) so as to at least cover the final bump structures 90'''. The initial epoxy layer 22 is preferably formed by spin coating, i.e. coating the epoxy onto the wafer/die/chip substrate 10 by means of spinning/rotary motion wherein the epoxy is poured onto the center of the wafer/die/chip substrate 10 with the aid of an epoxy volume dispenser or equivalent, and then spinning the wafer/die/chip substrate 10 to evenly distribute the epoxy over the wafer/die/chip substrate 10 and at least over the final bump structures 90''' to form initial epoxy layer 22.

Plasma Etch – Fig. 13

As shown in Fig. 13, the wafer/die/chip substrate 10 is placed in a plasma etching machine and a plasma etch is used to etch the initial epoxy layer 22 to a predetermined thickness, that is to:

etch epoxy layer 22 down to above the solder lines 14 to form final epoxy layer 22' of the first embodiment (see Figs. 1 and 2);

etch epoxy layer 22 down to below the solder lines 14 to form final epoxy layer 22'' of the second embodiment (see Figs. 3 and 4); or

etch epoxy layer 22 to form final epoxy layer 22''' that is above some solder lines (214'') and below other solder lines (214') (not shown in Figs. 13 to 15 for simplicity).

The plasma etch preferably employs oxygen and CF_4 (Tetrafluoromethane) ions. The plasma etch is conducted at the following parameters:

RF power: preferably from about 1000 to 1200 Watts; and more preferably from about 1000 to 1200 Watts; and

temperature: preferably from about 60 to 100°C; and time: preferably from about 15 to 20 minutes and more preferably about 15 minutes.

The completes formation of the epoxy coated 22'/22'' wafer/die/chip substrate 10 as shown in Figs. 13 and 14.

Sawing the Wafer/Die/Chip – Fig. 15

As shown in Fig. 15, the epoxy coated 22'/22'' wafer/die/chip of Fig. 14 is sawed to form completed wafer level-chip scale packages (WL-CSP) 100.

As discussed above, the final bump structures 90''' of the wafer level-chip scale packages (WL-CSP) 100 are preferably composed of two sets of final bump structures 90''': one having a first height (90'''A) and the other having a second height (90'''B) that is less than the first height (the third embodiment) for stacked die or multi-tier substrates (IC or MEMS applications).

This is more easily appreciated in Figs. 16 and 17 as now discussed.

Stack Die/Chip Mounting With Variable Height Bumps 90''' – Fig. 16

As shown in Fig. 16, utilizing the wafer level-chip scale packages (WL-CSP) 100 formed in accordance with the present invention having a first set of final bump structures 90'''A having a first height and a second set of final bump structures 90'''B having a second height that is less than the first height on a first chip (CHIP 1), a stack die/chip mounting is achieved.

As shown, the solder lines 14' of the first set of final bump structures 90'''A is above the top of the epoxy layer 22''' while the solder lines 14'' of the second set of final bump structures 90'''B is below the top of the epoxy layer 22'''.

Epoxy layer 22''' is preferably comprised of thermosetting resins or underfill coating material.

A second chip (CHIP 2) 50 is mounted to the second set of final bump structures 90'''B having the second, lower height so that it and the first chip (CHIP 1) are mounted flush with a substrate 60. As shown in Fig. 14, the second chip (CHIP 2) 50 is preferably mounted over the center portion of the first chip (CHIP 1).

Flip Chip Mounted to a Dual Height Substrate – Fig. 17

As shown in Fig. 17, a flip chip employing the dual height final bump structures 90'''A, 90'''B is mounted to a dual height substrate 62 wherein the lower

height portion 66 of the substrate 62 mounts to the first set of final bump structures 90'''A having a first height on the flip chip substrate 10' and the higher height portion 64 of the substrate 62 mounts to the second set of final bump structures 90'''B having a second height on the flip chip substrate 10' that is less than the first height.

As shown, the solder lines 14' of the first set of final bump structures 90'''A is above the top of the epoxy layer 22''' while the solder lines 14'' of the second set of final bump structures 90'''B is below the top of the epoxy layer 22'''.

Advantages of the Invention

The advantages of one or more embodiments of the present invention include:

1) fast process;

2) requires minimal tooling;

3) various bump shapes and sizes;

4) flexibility of two or more different bump heights;

5) better electrical and thermal performances; and

6) ease of design.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.